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GEB FifoOut 16

Variable width Output Fifo

Core Overview

The on-chip FIFO memory core buffers data and provides flow control in a system. The core operate with with separate clocks for the input and output ports. The minimum buffer size is one block of 512 entries, multiple blocks can be allocated at compilation time. Each entries are 16 bits wide and can be organized such as singles words or two bytes, allowing to use the fifo how a single 16 bits fifo, generating a 16 bit data flow or two byte wide indipendent fifos, able to generate two different data flow with different speeds and controls.

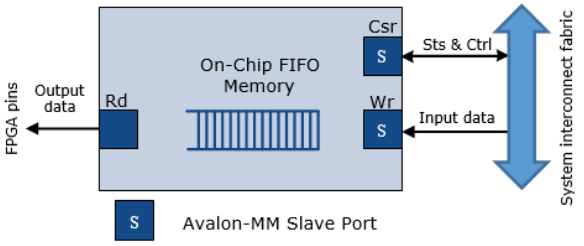
The FIFO appears on the bus in two different areas, one dedicated to the FIFO data and a second dedicate to manage and configure the FIFO, called CSR. The registers inside the CSR allow to select between byte wide and word wide organization, read the number of allocated blocks, read the number of words in the FIFO, manage the interrupt.

The FIFO data input interface is an Avalon-MM write only slave. The data is delivered to the output interface in the same order that it was received at the input interface. A status interface includes on CSR registers to set and control FIFO status and interrupts. Handshake signals are available to manage the data input flow and its backpressure, status and control bits allow the management of the output data flow.

The output FIFO I/O interface is compatible with the SMILE (Switch Matrix I/O Local Expansion) IP allowing the I/O configuration by PC application. The I/O configuration file can be also generated by the free FEWE tools (Fpga Easy Web Editor) provided by GEB Enterprise.

Functional Description

The input and output interfaces can use the optional backpressure signals to prevent underflow and overflow conditions. For the internal Avalon-MM interface, backpressure is implemented using the *fifo_full* status bit that must be polled before shift new data into the FIFO. On the external side, backpressure is implemented using the *fifo_empty* and *RdReq* signals available on the FIFO (Altera DCFIFO).

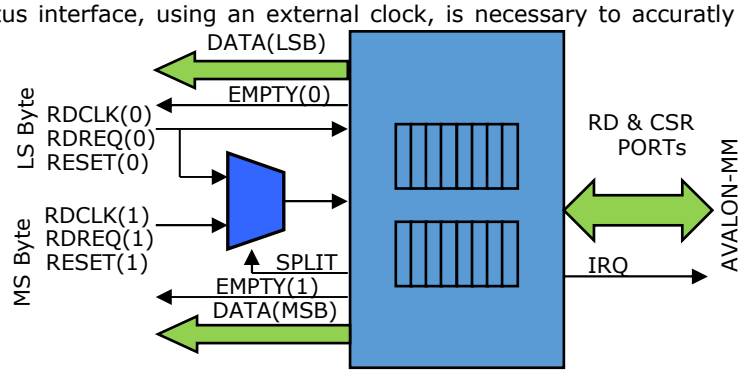


The FIFO has two interface on the Avalon internal side:

- WR port use to out the outgoing data, 8 or 16 bits wide, depending from the Byte/Word SPLIT Bit.
- CSR (Configuraion Space Register) port, 8 bits wide, read/write, used to control the FIFO status, the interrupt line, the Byte/Word SPLIT bit and so on.

External RD Port

In the used dual clocking scheme, a second status interface, using an external clock, is necessary to accuratly monitor the status of the FIFO output queue. This second interface isn't avilable to be controlled by internal bus, its data, controlls and status signals are bring out through the fpga pins to be menaged by external logics. Data and controls are separeted; there are a pairs of byte DataBus, WrClk, Wrq, Empty and Reset signals allowing the use such as two-byte wide fifos. When the FIFO is programmed to operate in 16 bits mode, only the LSB controlls will be used, the MSB one will be left unused.



WR Port

The WR port is 8 or 16 bits wide, it can grant two distinct single byte wide writes or one 16 bits write, allowing the FIFO to be used such as a single 16 bits FIFO or two byte wide FIFOs (FIFOL and FIFOH). In the CSR there will be status and controls registers for manage both fifos.

CSR Port

The FIFO core provides one CSR (Configuration and Status Interface) for the read master reading from the input interface. The CSR interface make available three registers:

- FO_STS, FO_CTRL, read status or write controlls of FIFO core.
- FO_CNF, fifo size in number of 512 bytes blocks -
- FO_USDWL, Number of used word in low fifo buffer.
- FO_USDWH, Number of used word in high fifo buffer.

IP External pins

The signals available on IP core pins are:

- DATA(15:0): Output Data bus from the Fifo
- RDCLK(1:0): Read Clock, active on rising edge, Read (shifts) DATA from the FIFO
- RDREQ(1:0): Read Request, a "1" enables the data Read. The new outcoming data will be available in the next clock cycle following the rising edge that has sampled RDREQ active.
- EMPTY(1:0): Status Empty of output Fifo, "1" when Empty
- RESET(1:0): Reset the Fifo, "1" to reset. Note that it has effect on the fifo array only, it does not reset the CSR registers conrol bits.

IRQ Generation

The FIFO core can be configured to generate an IRQ on certain conditions. The FIFO supports:

- OFNF1/0, Interrupt on fifo high/low not full. An interrupt will be generated when the FIFOL/FIFOH will have space for at least one byte in the buffer. A "1" on the corresponding OFIENF1/0 bit of the CSR register will be needed to allow interrupt generation.

Register Map

An Avalon-MM master peripheral, such as a CPU, controls and communicates with the FIFO core via two sets of registers, the RD port and CSR ports, either byte wide.

Base & Offset	Register Name	R/W	Descriptions		
WR+0	FO_DATA	R	Write and Shift the fifo Data.		
CSR+0	FO_STS	R	Fifo Input Status		
			D7	SPLIT	Fifo Split Bit: 1=Split, 2X8Bits. 0=Don't split, 1x16bits
			D3	OFIENF1	1=Enable Interrupt on Fifo high not full
			D2	OFIENF0	1=Enable Interrupt on Fifo low not full
			D1	OFNF1	1=Fifo high not full
			D0	OFNF0	1=Fifo low not full
CSR+0	FO_CTRL	W	Fifo Input Control		
			D7	SOFENF1	1=Set OFIENF1, Interrupt on Fifo high Not full
			D6	ROFENF1	1=Reset OFIENF1, Interrupt on Fifo high Not full
			D5	SOFENF0	1=Set OFIENE0, Interrupt on Fifo low Not full
			D4	ROFENF0	1=Reset OFIENE0, Interrupt on Fifo low Not full
			D3	OFSETSPLT	1=Set SPLIT Bit (2x8Bits Fifo will be active)
			D2	OFCLRSPLT	1=Clr SPLIT Bit (1x16Bits Fifo will be active)
			D1	OFCLR1	1=Reset Fifo High
			D0	OFCLR0	1=Reset Fifo low
CSR+1	FO_CNF	R	Fifo Configuration Register		
			D7-0	OFSIZE	Fifo Size in pages of 512 bytes.
CSR+2	FO_USDWL	R	Low Fifo used word		
			D7-0	USEDW	Used world, 255 value indicate 255 or more word in the fifo
CSR+3	FO_USDWH	R	High Fifo used word		
			D7-0	USEDW	Used world, 255 value indicate 255 or more word in the fifo

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