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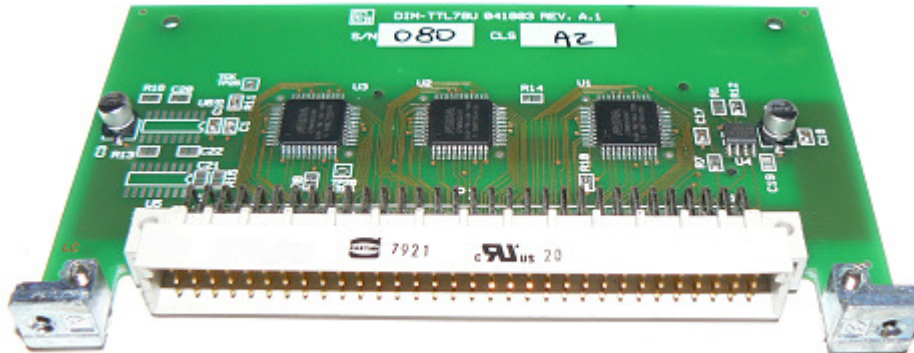
General Electronics Business

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**Digital Modules for Boundary
Scan Parallel I/O Access**

Model: BSPIO-78TTLU



Features

- 78 LVTTTL I/O channels for logic drive and sense
- High reliability DIN41612 I/O connector
- Reliable screw lock brackets
- Size 122mm X 70mm
- I/O organized in 3 segments of 26 pins each
- 96 bit Boundary-scan Register Length
- Each segment can be independently bypassed
- Medium-speed 10MHz TCK for high reliability at the best cost/performance ratio
- Each pin is independently programmable for sense, drive, bi-directional, and tri-state operation
- Fully-compatible JTAG/IEEE 1149.1 Test Access Port (TAP)
- Drives 3.3V logic, 5V tolerant
- Operating power 3.3V
- Fast, Low impedance, unprotected I/O channel driver can be used as a clock signal (*fast I/O drivers, at low impedance, without protection, can be used as clock signals*)
- Optional LVDS TCK interface can be used in large fixtures to avoid noise and skew problems.

General Description

The BSPIO-78TTLU provides bi-directional parallel-scan access to up to 78 TTL electrical nodes for the driving and sensing of logic values. This module increases the effectiveness of boundary-scan testing, enabling verification of all board connectors and within logic clusters. The BSPIO-78TTLU is available in two versions, both of them compatible with the standard DIN41612 female connectors in a test fixture. One version, the BSPIO-78TTLU-A1, is primarily intended for test fixtures with few BSPIOs, and contains a standard TTL interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using direct connection to the JTAG/IEEE 1149.1 Test Access Port (TAP). The other version, the BSPIO-78TTLU-A2, is intended for test fixtures with many BSPIOs and contains a balanced LVDS interface on the TAP's TCK signal. This module facilitates boundary-scan interconnection testing using a small interface connection to a JTAG/IEEE 1149.1 TAP.

Functional Description

Test and programming application development tools from JTAG Technologies support automatic integration of the BSPIO-78TTLU with the target board design by adapter file. This allows the inputs and outputs of the BSPIO-78TTLU to be driven and sensed via boundary-scan, thereby providing increased scan access to the target. The 78 channels of the BSPIO are grouped into three segments of 26 I/Os, each with its own boundary scan device, capable of operating at a 10 MHz TCK clock rate. Data is shifted in and out of all three segments in series. Each of the three segments may be placed into BYPASS mode, in which case scan data is shifted through the scan register of the segments that are used and the BYPASS registers in the other segments.

The TAP interface available on the DIN41612 connector is the actual test access port for the module. It can be used to daisy-chain the module to other BSPIO-78TTLU modules or to scan chain on the target board.

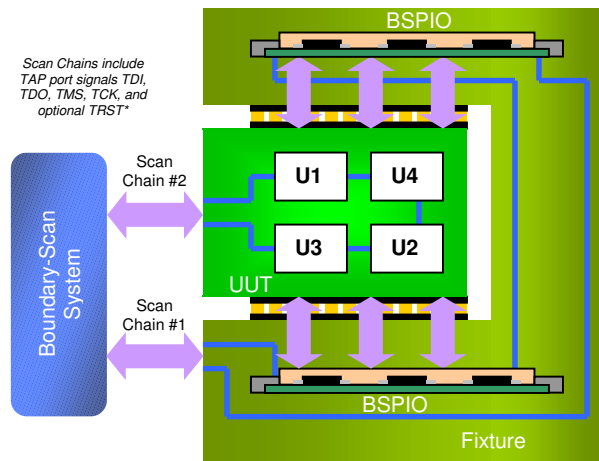


Fig.1 Use of the BSPIO-TTL78U on the Test Fixture

Specifications

Length of ID Register	32 bits per segment
Length of Boundary-scan Register	96 bits per segment, 3 segments
Maximum Shift Frequency	10MHz
I/O Channels (3 segments, 26 I/O each segment)	Input, output, bi-directional tri-state
Power Consumption	typ<40mA, max depending on the target I _{OH} and I _{OL}

DC Operating Conditions

Parallel I/O as Inputs	V _{IL} <0.8V V _{IH} >2.0V 5V tolerant, I _{IN} < 10 μA
Parallel I/O as Outputs	I _{OL} <8 mA, I _{OH} <8 mA drive 2.4V < V _{OH} < 3.3V, V _{OL} < 0.4V
TAP (*1)	All V _{IL} <0.8V V _{IH} >2.0V
TAP TCK(*2)	1<V _{OS} <1.65 -100mV<V _{TH} /V _{TL} <100mV

(*1) Not Applicable to TCK version A2

(*2) Applicable to TCK version A2

Ordering Information

GEB P.N.	Description
BSPIO-TTL78U-A1	78 LVTTTL I/O channels for logic drive and sense, TCK input LVTTTL level
BSPIO-TTL78U-A2	78 LVTTTL I/O channels for logic drive and sense, TCK input balanced LVDS level



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