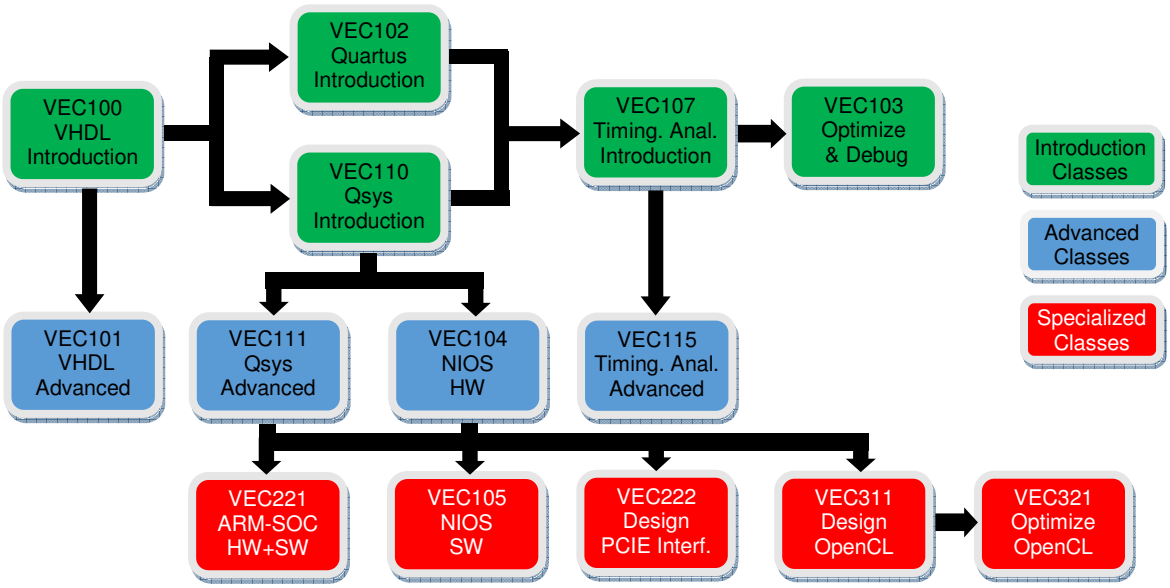
Intel® (formerly Altera®) Training Road Map



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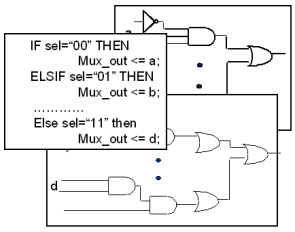
VEC100-Introduction to VHDL



This two-day course is a general introduction to the VHDL language and its use in programmable logic design. The emphasis is on the synthesis constructs of VHDL; however, you will also learn about the simulation constructs. You will gain a basic understanding of VHDL to enable you to begin creating your design file. In the hands-on laboratory sessions, you will put this knowledge to the test by writing simple but practical designs. You will also learn the basic instructions needed for operating both the synthesis and simulation tools of the Quartus® Prime software.

Course Duration: 2 Days

***At Course Completion* You will be able to:**

- Implement basic VHDL constructs
- Implement modeling structures of VHDL
- Behavioral
- Structural
- Use VHDL building blocks (Design Units)
- Entity
- Architecture
- Configurations
- Package declarations
- Package bodies
- Create projects in Quartus Prime software
- Perform simulation in the Quartus Prime simulator

Skills Required

- Background in digital logic design
- Knowledge of simulation is a plus
- Prior knowledge of a programming language (e.g., "C" language) is a plus
- No prior knowledge of VHDL or Quartus Prime software is needed

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VEC102-QUARTUS Prime: Foundation

You will learn how to use the Quartus® Prime software to develop an FPGA or CPLD. You will create a new project, enter in new or existing design files, and compile your design. You will also learn about timing constraints and analyze a design compiled with these constraints using the TimeQuest timing analyzer, the path-based static timing analysis tool included with the Quartus Prime software. You will learn techniques to help you plan your design. You will employ Quartus Prime features that can help you achieve design goals faster. You will also learn how to plan and manage I/O assignments for your target device.

Course Duration: 2 Days

***At Course Completion* You will be able to:**

- Make pre-project decisions to plan design
- Create, manage & compile Quartus Prime projects
- Plan & manage device I/O assignments using Pin Planner
- Assign clock & I/O constraints to improve design performance
- Analyze clock & input/output timing using TimeQuest
- Review compilation results

Skills Required

- Background in digital logic design
- Ability to describe a hardware system using VHDL, Verilog or EDA schematic tool
- Experience with PCs and the Windows operating system

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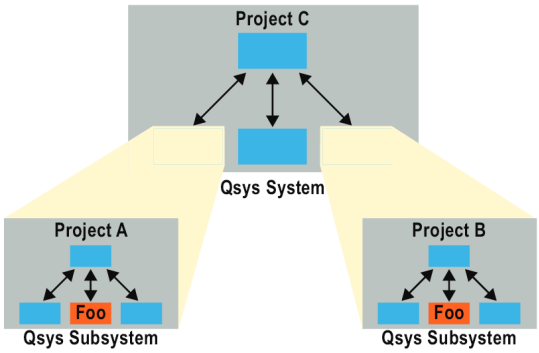
VEC110- Introduction to the Qsys System Integration Tool

This class will teach you how to quickly build designs for Intel® FPGAs using Intel's Qsys system-level integration tool. You will become proficient with Qsys and will expand your knowledge of the Quartus® Prime FPGA design software. You will learn how to build hierarchical systems, how to quickly integrate IP and custom logic into a system, and also how to optimize designs for performance. Since Qsys makes design reuse easy through standard interfaces, we will dive deeply into the Avalon-Memory Mapped and Streaming Interfaces. The class provides a significant hands-on component, where you will gain significant exposure to tool usage as well as system and custom HDL component design.



Course Duration: 3 Days

***At Course Completion* You will be able to:**

- Utilize key features of Qsys, understand files produced & how they fit into the project hierarchy
- Build digital systems
- Exploit Qsys' hierarchical capability to add flexibility & scalability to your design
- Create custom components with Avalon-MM / Avalon-ST interfaces
- Test custom components with the Avalon Verification Suite (or Bus Functional Models) in the ModelSim simulator
- Perform in-system diagnosis & control via System Console
- Integrate CPU subsystems into a project

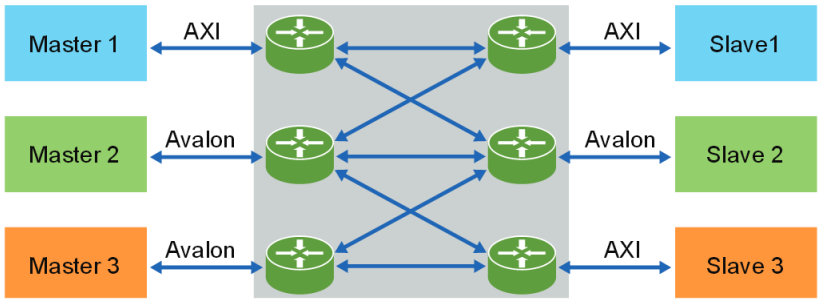
Prerequisites

We recommend completing the following courses:

- The Quartus Prime Software Design Series: Foundation

Skills Required

- Background in digital logic design
- Working knowledge of the Quartus Prime design software
- Knowledge of HDL coding methodology (helpful but not mandatory)



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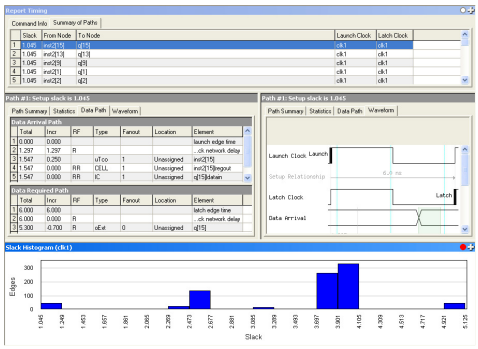
VEC107-QUARTUS Prime: Timing Analysis

You will learn how to constrain & analyze a design for timing using the TimeQuest timing analyzer in the Quartus® Prime software. This includes understanding FPGA timing parameters, writing Synopsys Design Constraint (SDC) files, generating various timing reports in the TimeQuest timing analyzer & applying this knowledge to an FPGA design. Besides learning the basic requirements to ensure that your design meets timing, you will see how the TimeQuest timing analyzer makes it easy to create timing constraints to help you meet those requirements.



Course Duration: 2 Days

***At Course Completion* You will be able to:**

- Understand the TimeQuest timing analyzer timing analysis design flow
- Apply basic and complex timing constraints to an FPGA design
- Analyze an FPGA design for timing using the TimeQuest timing analyzer
- Write and manipulate SDC files for analysis and controlling the Quartus Prime compilation

Prerequisites

We recommend completing the following courses:

- Quartus Prime: Foundation

Skills Required

- Experience with PCs and the Windows operating system
- Completion of "The Quartus Prime Software Design Series: Foundation" online or instructor-led course OR a working knowledge of the Quartus Prime software

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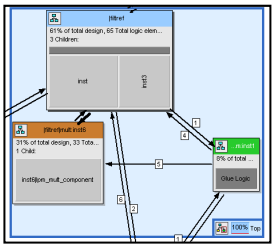
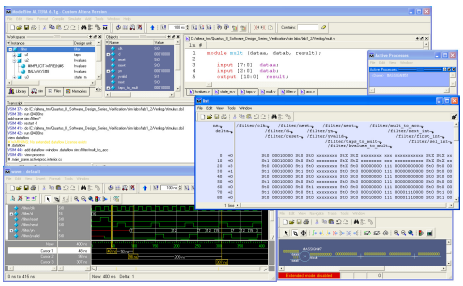
VEC103-QUARTUS Prime: Verification & Optimization



You will learn features of the Quartus® Prime software that will enable you to verify your FPGA design and will enable you to shorten your design cycle as well as improve your design performance and utilization.

Verification: You will learn how to simulate Intel® IP and megafunctions in other EDA simulation tools. You will also estimate FPGA power consumption using tools found in the Quartus Prime software. You will use debugging tools available in the Quartus Prime software, such as the SignalTapII® embedded logic analyzer, In-System Sources & Probes, & the Logic Analyzer Interface. You will learn to select the correct tool to effectively debug your design.



Optimization: You will use the incremental compilation flow and LogicLock™ regions in the Quartus Prime software to reduce compile times and preserve performance on selected regions of your designs. You will obtain your design goals in the area of performance, resource usage and power consumption by using design strategies, HDL coding styles and Quartus Prime software settings. You will also learn how to manage compile times effectively.

Course Duration: 3 Days

***At Course Completion* You will be able to:**

- Analyze power consumption with the PowerPlay power analyzer
- Debug designs in-system using the SignalTap II embedded logic analyzer
- Connect internal debug nodes to an external logic analyzer using the Logic Analyzer Interface
- View & edit embedded memory contents using the In-System Memory Content Editor
- Make incremental design changes with Chip Planner
- Define physical region constraints for an FPGA design using LogicLock regions
- Manage user-defined design partitions using the Quartus Prime incremental compilation flow
- Apply incremental compilation to the top-down & bottom-up design flows
- Use Quartus Prime software settings to improve internal & I/O timing, reduce logic resource usage & lower power consumption
- Choose recommended HDL coding styles
- Run Design Space Explorer to select optimal setting for full or partial designs

Prerequisites

We recommend completing the following courses:

- QUARTUS Prime: Foundation
- QUARTUS Prime: Timing Analysis

Skills Required

- Experience with PCs and the Windows operating system
- Completion of "The Quartus Prime Software Design Series: Foundation" course OR a working knowledge of the Quartus Prime software
- Completion of "The Quartus Prime Sotware Design Series: Timing Analysis" course OR a working knowledge of Synopsys Design Constraints (SDC) and the TimeQuest timing analyzer

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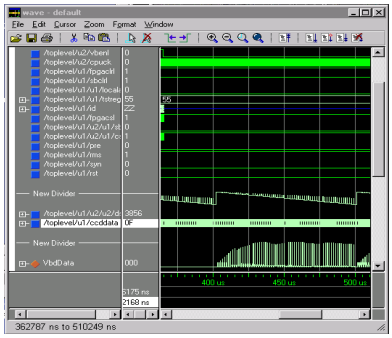
VEC101-Advanced VHDL Design Techniques



In this course, you will learn & practice efficient coding techniques for VHDL synthesis. You will gain experience writing behavioral & structural code & learn to effectively code common logic functions including registers, memory & arithmetic functions. You will use VHDL constructs to parameterize your designs to increase their flexibility and reusability. While the concepts presented will mainly be targeting Intel® devices using the Quartus® Prime software environment, many can be applied to synthesizing hardware using other synthesis tools as well. You will also be introduced to testbenches, VHDL constructs used to build them & common ways to write them. The hands-on exercises will use Quartus Prime software to process VHDL code and ModelSim®-Intel® software for simulation.

Course Duration: 2 Days

***At Course Completion*You will be able to:**

- Develop coding styles for efficient synthesis when:
- Targeting device features
- Inferring logic functions
- Using arithmetic operators
- Writing state machines
- Use Quartus Prime software RTL Viewer to verify correct synthesis results
- Incorporate Intel® structural blocks in VHDL designs
- Write simple testbenches for verification
- Create parameterized designs

Prerequisites

We recommend completing the following courses:

- Introdution to VHDL

Skills Required

- Completion of the "Introduction to VHDL" course or some prior knowledge and use of VHDL
- Strong background in digital logic design
- Understanding of synthesis and simulation processes

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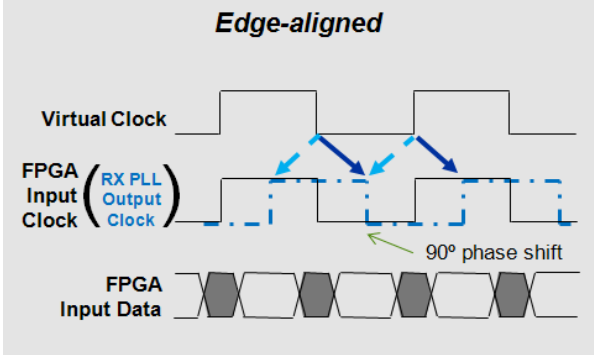
VEC125-QUARTUS Prime: Advanced Timing Analysis with TimeQuest

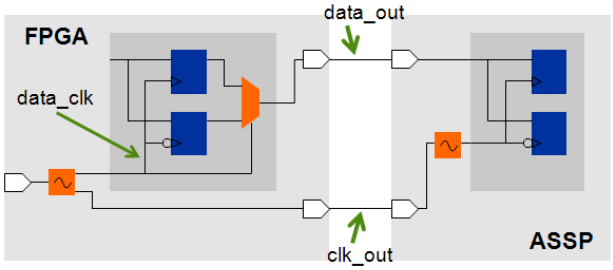
Using the Quartus® Prime software and building upon your basic understanding of creating Synopsys Design Constraint (SDC) timing constraints, this class will guide you towards understanding, in more depth, timing exceptions. You will learn how to apply timing constraints to more advanced interfaces such as source synchronous single-data rate (SDR), double-data rate (DDR) and LVDS, as well as clock and data feedback systems. You will discover how to write timing constraints directly into an SDC file rather than using the GUI and then enhance the constraint file using TCL constructs. You will also perform timing analysis through the use of TCL scripts.



Course Duration: 3 Days

At Course Completion *You will be able to:*

- Write Tcl script files to automate constraining and analysis of FPGA designs
- Apply timing exceptions to real design situations
- Properly constrain and analyze the following design situations: source synchronous interfaces, external feedback designs, and high-speed interfaces containing dedicated SERDES hardware



Prerequisites

We recommend completing the following courses:

- The Quartus Prime Software Design Series: Foundation
- The Quartus Prime Software Design Series: Timing Analysis

Skills Required

Experience with PCs and the Windows operating system
Completion of "The Quartus Prime Software Design Series: Timing Analysis" course OR a working knowledge of the TimeQuest timing analyzer and basic SDC commands

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VEC104-NIOS II and QSYS

This course will teach you how to design in a soft core embedded processor with an Intel® FPGA. This course is focused on the hands-on development of Nios II hardware using the Nios II Development Kit. You will learn how to integrate a Nios II 32-bit microprocessor and test it in an Intel® FPGA. You will learn how to configure and compile designs using the Quartus Prime software and QSYS. You will participate in discussions about the features and capabilities of the development board along with how to create and test your own custom IP or custom Instruction. The training is hardware designer oriented with some hint on HAL driver design and software design in the Eclipse enviroment. After taking this course you should feel confident tackling your next SOPC design

Course Duration: 3 Days

At Course Completion You will be able to:

- Configure & compile a Nios II design using QSYS & Quartus Prime software
- Compile, run, & debug embedded software
- Verify your design with the Quartus Prime, ModelSim®-Intel®, & Nios II IDE software
- Use Qsys to incorporate custom peripherals & instructions
- Build custom Avalon master or slave IP
- Create a custom instruction
- Utilize Avalon-MM & Avalon-ST interfaces
- Learn to access peripherals from C using the HAL API functions
- Reduce code size with system library properties
- Create interrupt-driven C code
- Access custom instruction hardware from C code

Prerequisites

We recommend completing the following courses:

- QUARTUS Prime: Foundation

Skills Required

- Background in digital logic design
- Working knowledge of the Quartus Prime design software
- Some knowledge on describing hardware in VHDL

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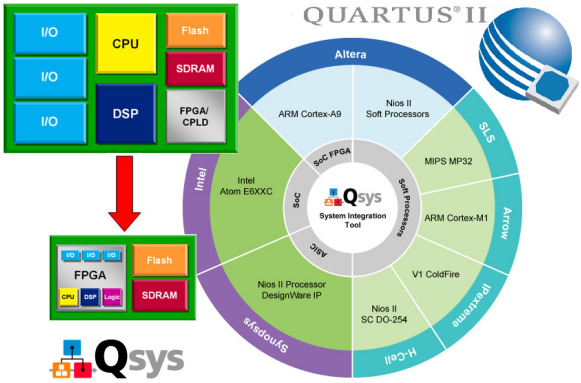
VEC105-Developing Drivers for the NIOS II



This course is targeted at Software Engineers or Developers. You will learn to develop and run embedded software for the Nios II processor Software Build Tools for Eclipse and with the Nios II Command Tools. You will also learn how to write new device drivers for custom peripherals and publish them the way that they can be successfully used inside new NIOSII projects.

Course Duration: 1 Day

***At Course Completion* You will be able to:**

- Create software project from hardware design deliverables
- Manage software projects using the Nios II IDE & Command Tools

Skills Required

- Some knowledge of programming in C, especially for embedded systems
- Basic understanding of hardware design in FPGAs
- Completion of the "VEC104: NIOS II and QSYS" course is optional but strongly recommended
- Build new device drivers for custom peripherals
- Publish new device drivers and use them inside new projects

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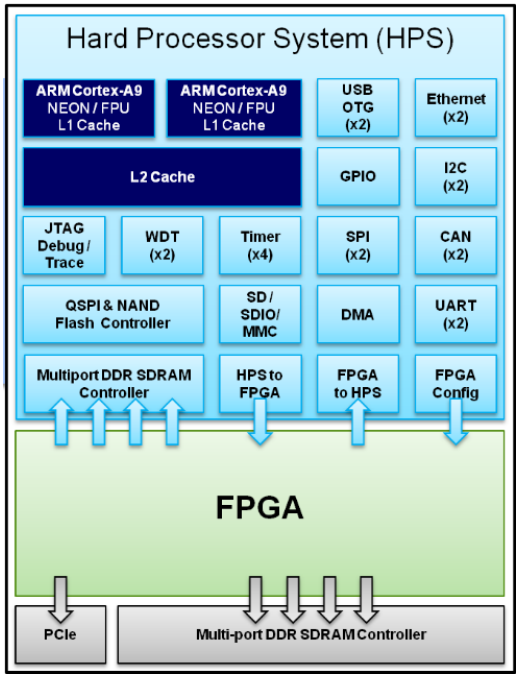
VEC221-Designing with an ARM-based SoC

This course is intended for hardware and firmware engineers and will leverage your knowledge of Qsys system design to guide you on implementing an Intel® SoC with the ARM® Cortex A9 hard processing system (HPS). This course focuses on the hardware aspects of using the processor in the SoC from the design, verification and debug hardware perspectives just as if the processor was external. Our intention is that you feel completely comfortable using the HPS in the SoC and know all of the resources at your disposal to work with the board designer, FPGA engineer, firmware engineer or software engineer to get up and running quickly.



Course Duration: 2 Days

***At Course Completion* You will be able to:**

- Create, manage, and compile an SoC in the Qsys tool
- Simulate the HPS component as part of a Qsys system using Mentor Graphics Modelsim® tool
- Bring up and debug an SoC with the System Console tool
- Cross trigger between the FPGA and ARM processors using the SignalTap II logic analyzer
- Explain the hardware to software file handoff
- Design with the Golden reference design on the Cyclone V SoC development kit

Prerequisites

We recommend completing the following courses:

- Advanced Qsys System Integration Tool Methodologies
- Introduction to the Qsys System Integration Tool

Skills Required

- FPGA knowledge is not required, but a plus

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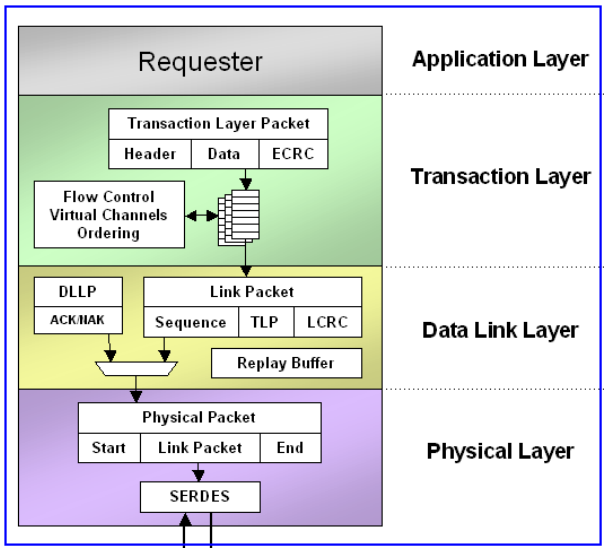
VEC222-Creating PCI Express Links Using FPGAs

Are you beginning or working on a design that uses one or more PCI Express® interfaces? Do you have questions regarding bringing up your FPGA's PCIe® link? Then this course should be of interest to you!
We'll start with a high-level overview of the PCI Express protocol and from there you'll learn the design flow to target the Hard IP for PCI Express blocks found in Cyclone® V, Arria® V and Stratix® V devices, particularly when using the Qsys system design tool. You'll see how to debug and test your PCIe links, both through simulation and in-system. You'll discover advanced device features to add more flexibility and capability to your PCI Express-based design. By the end of the training, you'll feel comfortable getting your own device's PCIe link up and running.



Course Duration: 2 Days

At Course Completion You will be able to:

- Describe the features and functionality of the Hard IP for PCI Express.
- Build a PCI Express solution targeting an FPGA using the Qsys system development tool
- Generate a testbench to simulate the Hard IP for PCI Express and modify the testbench to perform custom tests
- Debug a PCIe link using Intel® debugging tools and transceiver features

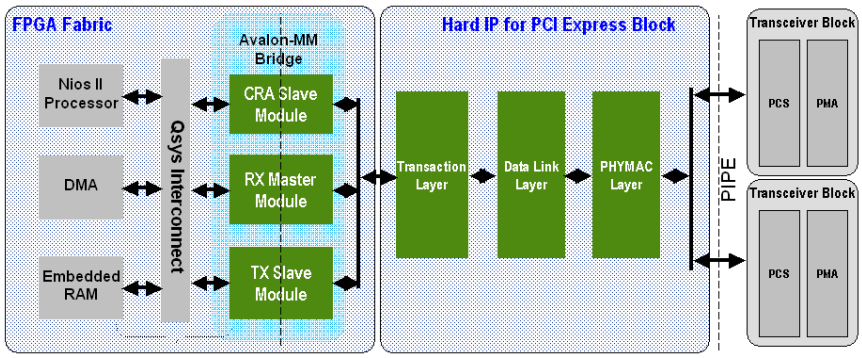
Prerequisites

We recommend completing the following courses:

- The Quartus Prime Software Design Series: Foundation
- Transceiver Basics

Skills Required

- Some understanding of the PCI Express Protocol specification is helpful, but not required
- Familiarity with common high-speed transceiver architecture.
- Familiarity with FPGA/CPLD design flow
- Familiarity with the Quartus Prime design software
- Some familiarity with the Qsys design tool is helpful, but not required



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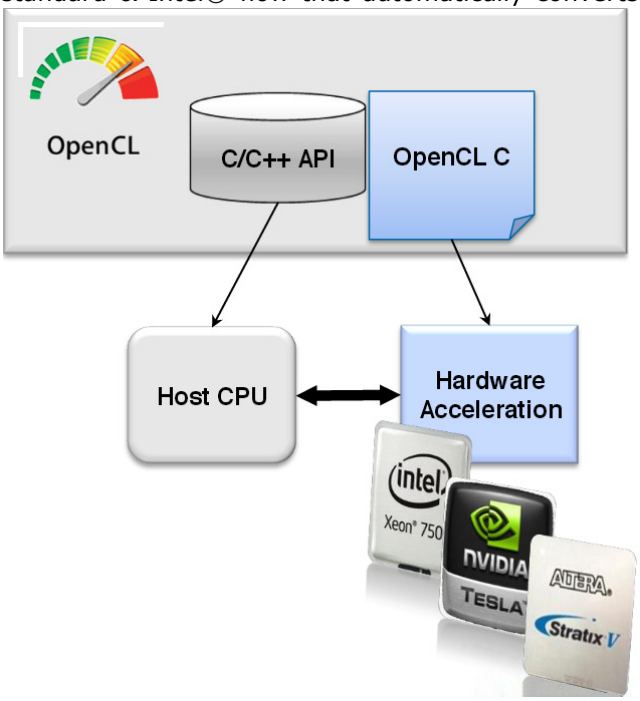
VEC311- Parallel Computing with OpenCL

OpenCL is a standard for writing parallel programs for heterogeneous systems. In the FPGA environment, OpenCL constructs are synthesized into custom logic. This course introduces the basic concepts of parallel computing. It covers the constructs of the OpenCL standard & Intel® flow that automatically converts kernel C code into hardware that interacts with the host. In hands-on labs, you'lll write programs to run on both the CPU & FPGA. Note.
This hands-on workshop provides an introduction to OpenCL for FPGAs. For in-depth training on OpenCL & Intel's OpenCL for FPGAs solution attend the "OpenCL for Intel® FPGAs" class from an ATPP partner.



Course Duration: 2 Days

At Course Completion You will be able to:

- Describe high-level parallel computing concepts and challenges
- Understand the advantages of using Intel's OpenCL solution
- Know the basics of the OpenCL standard
- Write simple programs in OpenCL
- Compile and run OpenCL programs using the Intel® solution

Skills Required

- Basic understanding of the C programming language

Follow-on Courses

Upon completing this course, we recommend the following courses:

- **VEC321** Optimizing OpenCL for Intel's FPGAs

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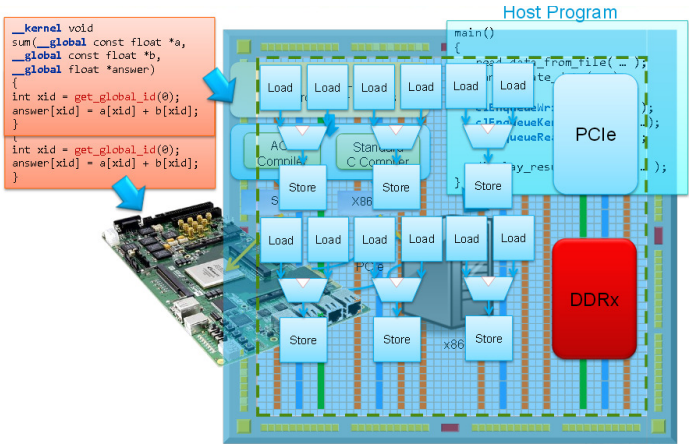
VEC321- Optimizing OpenCL for Intel® FPGAs

This course covers the optimization techniques needed to implement a high performance OpenCL solution on an FPGA using the Intel® SDK for OpenCL. We will discuss good coding design practices, ways to improve data processing efficiency, memory access efficiencies, and host side optimizations. We will also focus on Intel®SDK for OpenCL specific features that can significantly improve OpenCL performance on FPGAs compared to other platforms.



Course Duration: 2 Days

At Course Completion You will be able to:

- Use good coding design practices to implement a high performance OpenCL FPGA system
- Apply multiple methods to improve data processing efficiency of OpenCL kernels
- Improve memory access efficiencies in the system
- Optimize host side operations
- Understand Intel® specific features that will significantly boost the performance of an OpenCL solution

Prerequisites

We recommend completing the following courses:

- **VEC311** Parallel Computing with OpenCL

Skills Required

- Attendance of the Parallel Computing with OpenCL Workshop or a good understanding of the OpenCL standards

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