GEB Enterprise S.r.l.
General Electronics Business

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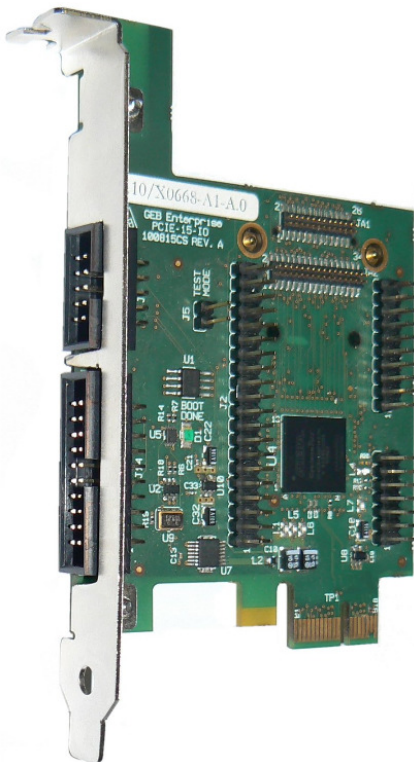
SOPC
System On Programmable Chip

PCI Express: PCIE-15-IO

GEB High Performance System On Card (Sopc-Card) product includes, all-in-one, whatever is needed to start using the advanced features of Altera CycloneIV-GX family and features a socketed board with an **EP4CGX15 or EP EP4CGX30**.

Features

PCIe

- PCI Express (PCIe) standard size
- Up to 53 user I/O digital channels, 3.3V LVTTL standard, each one with independent sense, drive, bi-directional, and tri-state capabilities.
- Up to 2 user output clocks signals (1 with dedicated PLL), 3.3V LVTTL standard.
- One user input clocks signal, 3.3V LVTTL standard, with dedicated PLL
- Single 3.3 V power supply voltage.
- Connectors (x1):
   - Medium density, 2X Samtech FTS-1XX-02-F-DV 1,27mm pitch on top sided
   - Altera Santa Cruz connectors set (J11-J12-J13) interface, 3.3 V input tolerant and 3.3V output capable.
   - Low density (100mills) 20pins J14 connector on front panel with 16 I/O, clocks, and wake up signals
- Wake up support
- User available FPGA resources in EP4CGX30 version [*1]:
   - Logic Element: 29440LE (14400LE)
   - Ram: 1080 Kbits (540Kbits)
   - PLL : 4 (3)
   - 18x18 bit multipliers: 80 (none)
- Boot device
- 1 Power supply monitor and reset circuitries.
- One Test Access Ports (TAPs).
- On board crystal oscillator
- Fully-compatible to JTAG/IEEE 1149.1 boundary-scan standard
- Altera USB blaster connector on front panel

(*1) User I/O connectors are available on the top, on the bottom, and on the front side.

Description

GEB PCIe Fpga card is the flexible solution to interface many equipments to a PC. The make it easy, a two pieces solution has been applied, splitting the interface on two boards.

- The first one will achieve logic function, it will be made by P CIE FPGA card that, appropriately programmed, will host the protocols of interface, standard or custom, serial or parallel, RZ, NRZ, Manchester, HDLC.... everything you would like to have
- The second one will be daughter board, a simple electrical interface board. It will host the glue logic needed to meet the interfaced system specification, RS232, RS422, RS485, LVDS, +28V discrete, opto coupled, and so on
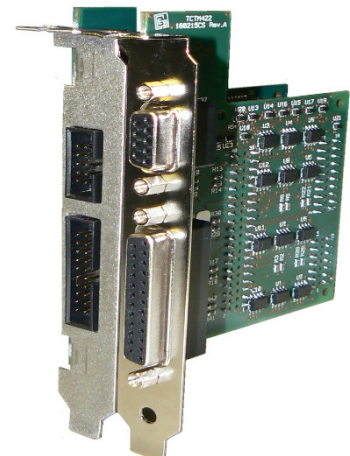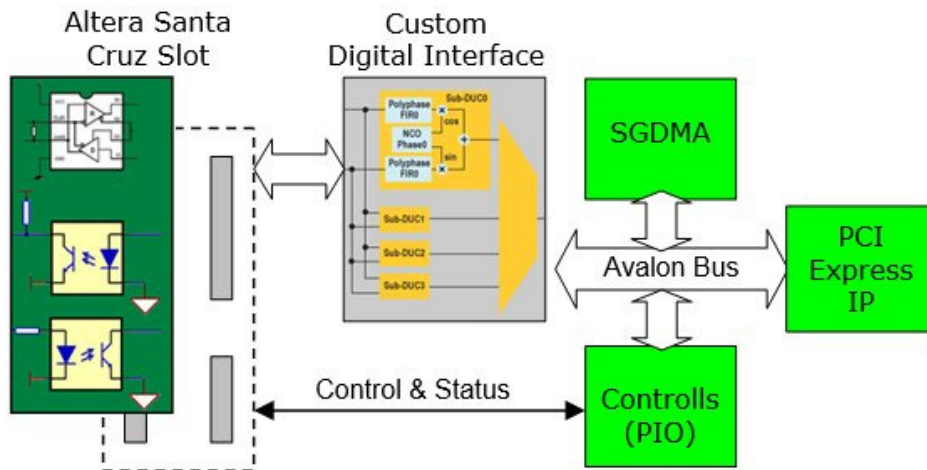
PCIe Fpga card allows an easy building of customized interfaces to be used on the PC, such as serial synchronous HDLC, RS422, RS485, optional high speed DMA:

- You can build a single slot sandwich with doughter board, placing its connectors on a PC bracket fitted in an empty slot. The signals would be brought to the connectors by a flat cable, how typically occur on many PC card.
- In addition, you can build a double slot sandwich, placing the I/O connectors directly on the daughter board (see the photo on the right).
- Finally, you could put an Intel (Altera) Santa Cruz daughter board; it can be hosted on PCIe Fpga board to build a fast prototype.

It is also available a programming interface on the board support in-system programming (ISP) using Altera USB Blaster.

The FPGA hardware design can be easily designed by Intel (Altera) QSYS system editor where modules written by VHDL, HLS (SystemC), schematic and AHDL can be combined to build your custom application.
QSYS systems designed to a GEB PCIe card may be fitted on all GEB PCIe boards family without any major changes.

The drivers supports PCIe interface under Windows and Linux O.S. Development kits make available examples of systems, master and target. Starting from them a custom system can be built in few hours.

The expansion J1-J3 connectors allow easy interface with AD/DA or others suitable interface placed on daughter boards. DSP and QSYS builders, allow DSP preprocessing, data management and high-speed data transfer from/to the host virtual memory.
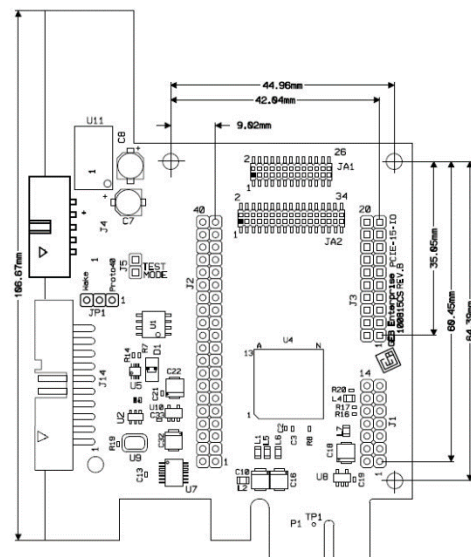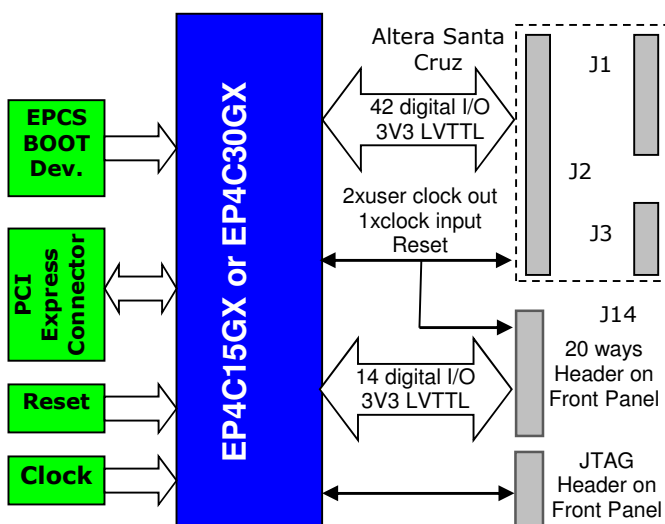
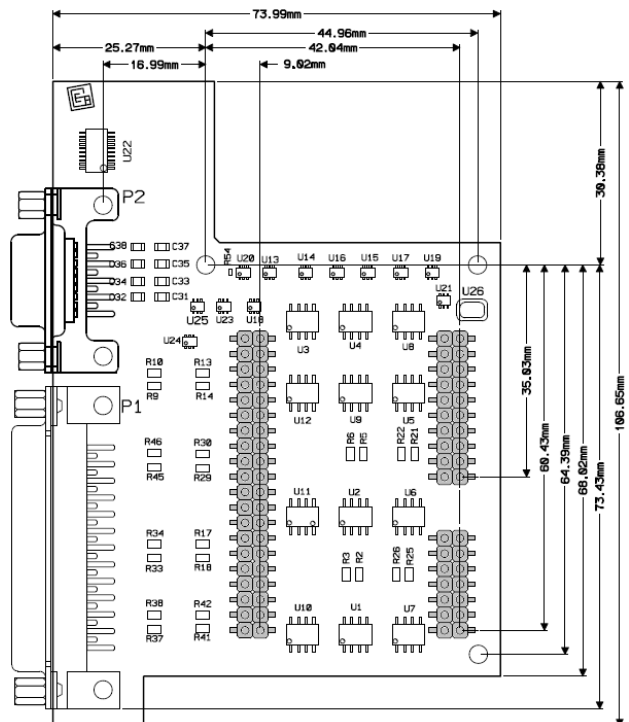The fpga signals available on J1-J3 connectors are 3V3 tollearant.
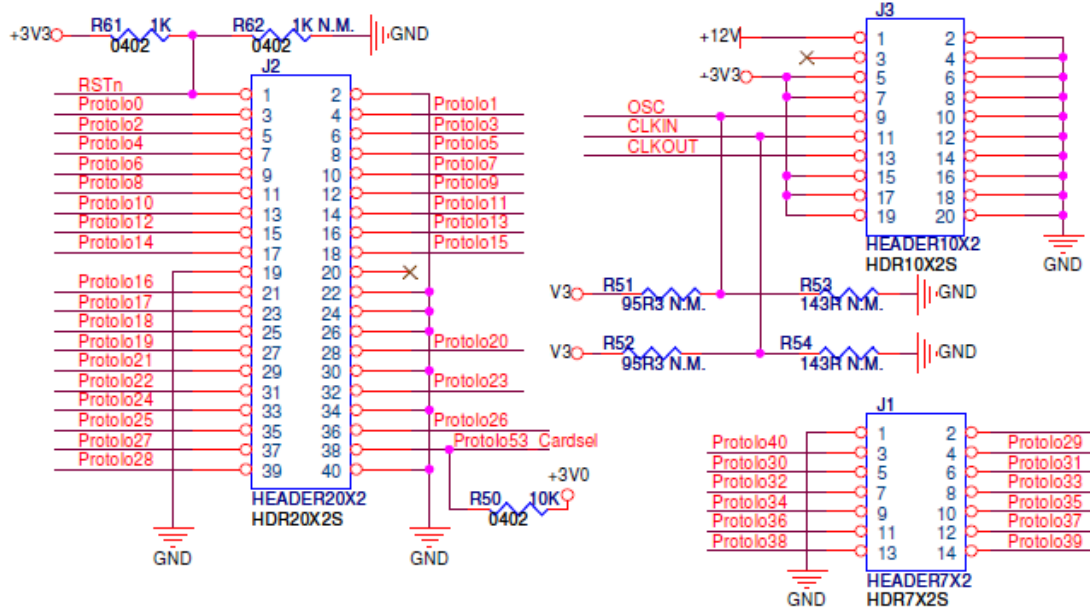
The Santa Cruz J1-J3 connectors are headers, male, 2.54mm pitch. The terminals length depends from the board version:
- Versions that hosting a daughter board will occupy one PC slot will be equipped with connectors like to Samtec TSW-1XX-07-F-D, the terminal height from top of pcb will be 8.4mm (330 mills)
- Versions that hosting a daughter board will occupy two PC slots will be equipped with connectors like to Samtec TSW-1XX-12-G-D, the terminal height from top of pcb will be 28.5mm (1.12Inchs)

In both case the suggested female header family of connectors that can be used on the daughter board is Samtec BCS-1XX-L-D-PE one. This kind of connectors, fitted on bottom side of the daughter board, will allow a great flexibility when to will be needed to adjust the height oh the boards sandwich.

Three 3.2mm holes allow fixing the daughter board by M3 screws and spacers.

The picture on the left shows an example of a daughter board that using the santa cruz connectors and that will use to two PC slots. The connectors J1-J3, in gray, should be placed in the bottom side og the board, in the picture them have been made visible to clarifly the parts placement and their distances.
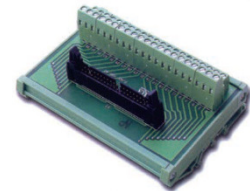
The Fpga I/O signals are present on others connectors:
- On J14, available on the front panel, that is a 20 ways header, 2.54mm pitch
- On JA1-JA2, placed on the board top side, 1.27mm pitch
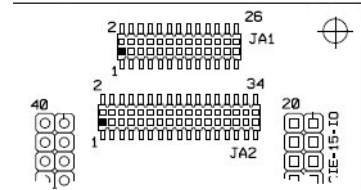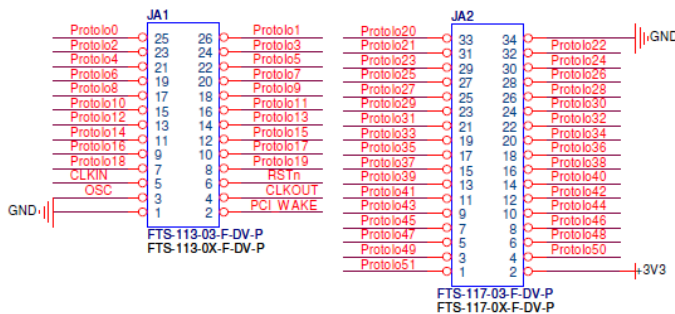
All of them shares the FPGA I/O signals available on J1-J3 connectors. JA1 and JA2 are Samtect FTS-11X-01 connectors that match with Samtec FFSD cables, allowing another one way to interface the application. The electrical interfaces devices can be fitted on a mechanical separeted board, toghether non-standard PC connectors, connected to Fpga board by a FFSD cable.

Application

A typical application of the product is the control of an I/O sub-system by a standard PC. The flexible and reconfigurable FPGA included in the product allows interfacing to all types of actuators and sensors with, or without, the optional support of the user defined firmware running on a NIOSII core. Moreover, it is also possible implementing in the FPGA a DSP pre-processing, with or without DMA support for data transferring to/from system memory. Moreover, the NIOSII soft core executes custom defined instructions that, together with a very fast interrupts response time (ranging between 1µs and 2µs), allows the user to achieve high demanding processing/time critical requirements, as requested by:
- Industrial Automation
- Electromedical applications
- Electromechanical applications
- Fast Data acquisition systems with hardwired integrated Digital Signal Processing

Specifications and Operating Conditions

Digital I/O levels	Vol = 0.4 V max., Voh = 2.4 V min., Vil = 0.8 V max., Vih = 2.0 V min.
Power supply voltage (current)	3.3 V +/- 5% (0.25A Typical, 0.6A Max) (*2)
Operative temperature range	-40 / + 85 ℃
Storage temperature range	-40 / +150 ℃

(*2) The current values depends from the configuration file loaded inside FPGA. The typical value was measured on typical application (100MHz system clock, 50% resource usage, 20% I/O switching at 10MHz). Maximum value was estimated using Altera tools in many large and fast designs. The maximum current values allowed depends also from the thermal resistance of the package and from the operating temperature

Ordering Information

Product Name	GEB Code	Description
PCIE-15-IO	100815A1	Basic low cost version equipped with EP4CGX15BF14C8N Fpga
PCIE-15-IO	100815A2	Version equipped with EP4CGX30BF14C6N Fpga and header connectors high 8.4mm. (Single slot board sandwich)
PCIE-15-IO	100815A3	Version equipped with EP4CGX30BF14C6N Fpga and header connectors high 28.8mm. (Two slots board sandwich)