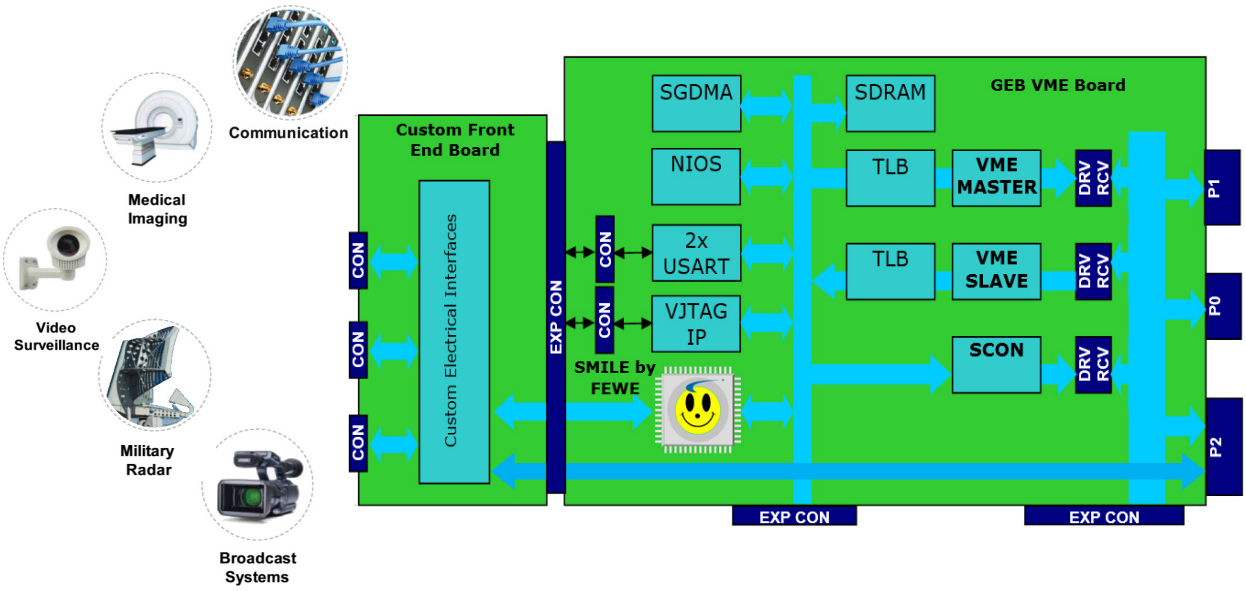
GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

VME-RDK
System On Programmable Chip

VME BUS Master/Slave Back End

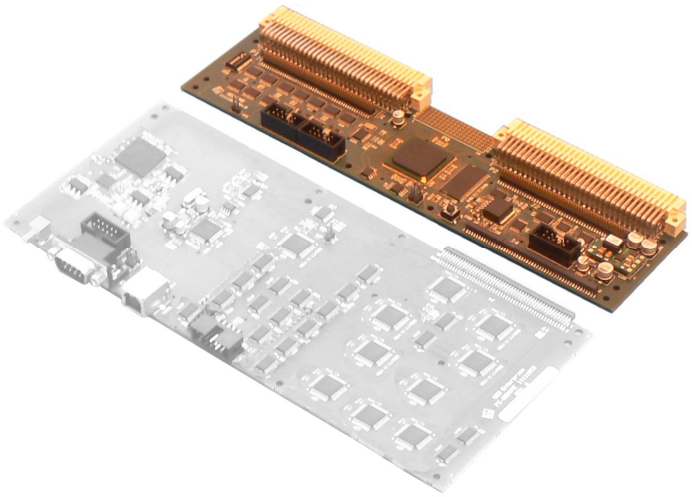
Overview

The GEB-VME board has the target to make available at low cost the resources to build a fast prototype of a VME master/slave/controller subsystems. The modularity of the resources, hardware in the board, firmware in the NIOS code and IP blocks, written in VHDL language, allow composing with **many types of applications with a low effort**.



The Two pieces solution

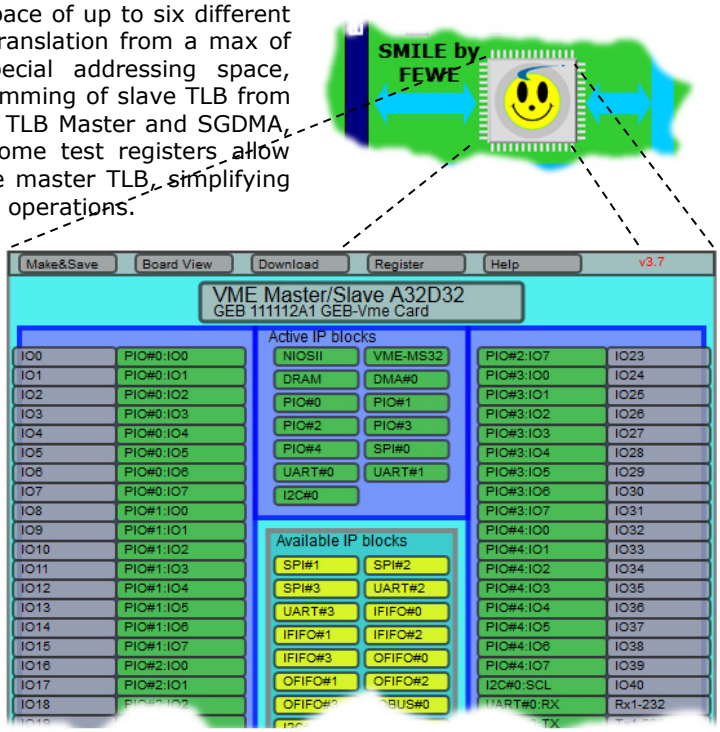
With the standard VME size of 233x160mm the application board will be built using two pieces solution composed by semi-boards. The first one is the GEB-VME, wide about 233x60mm shown on the right side of the figures who carries the Fpga that host VME IP and its related logic, the VME Drivers/Receivers, the SdRam and some ancillary logic, including a switching power supply, able to generate onboard 3.3V when it isn't available on the P0 connector. The GEB-VME also hosts an expansion connector (J4) and space for four smalls brackets needed to vigorously join into it to the second piece of the "Front End" board. An example of Front End Board is shown on the left side of the figure and has a size of about 233x100mm. The Fpga I/O signals,(about 44), are carried out from the GEB-VME P4 connector, a 100 way 1.27mm connector. The front-end board must be designed by customer to meet their own application will host the interface logic, controllers of simples level translator needed to establish the correct electrical and logical protocols required from external peripherals.



The current VME IP and NIOS firmware supports A32D32 master/slave cycles, interrupt handler, interrupter and SysCon. The related firmware (Monitor), running on NIOSII, allows the user to start all kind of buses cycles and some macro commands, such as memory test, using RS232 or USB data link.

VME IP Architecture

The IP Architecture allows the user to build many VME board structures. Building the user system is very simple: the local IP Bus is compliant to the Altera SOPC/QSYS specifications, allowing the users to make the FPGA subsystem using the Altera tools. The TLB Master Block allows the address translation from a local address to a Vme address, using an addressing space of up to six different VME addresses. The TLB Slave Block allows the translation from a max of six Vme addresses to a local address. A special addressing space, configurable at compilation time allows the programming of slave TLB from VME bus, opening the internal registers, including TLB Master and SGDMA, to be programmed by standard VME cycles. Some test registers allow access to all VME space without programming the master TLB, simplifying the access to VME resources during debug and test operations.



One of the External Bus I/F available is the SMILE (Switch Matrix Interfaces Logic Extensions) block. This allows the routing to many resources, starting from a programmable bus interface (an IP called IOBUS), up to standard peripherals controllers, such as UART, input FIFO, output FIFO, I2C, SPI and so on. Both the IOBUS and the peripherals have been available through the Fpga Pins on the J4 connectors. About 44 LVTTL signals have been available; all of them can be routed to the IP hosted in the FPGA through the SMILE switch matrix. The SMILE control file is needed to obtain the customized I/O configuration, it can be generated using the WEB tools [*1]. This control file could be applied by local NIOS firmware or by another host, resident on VME bus, using the VME slave port.

Different custom versions of external interface for specific application can be developed by GEB or by user, using Altera's tools, such as QuartusII and SOPC Builder or QSYS.

VME Compliance Levels

Features	Compliances
A32,A24,A16 Addressing Spaces	Supported
D32,D16,D8E,D8O Data Transfer	Supported
Master/Slave Block Transfer D64, D32, D16	Supported by hardware (Optional IP version)
Interrupter, Interrupt handler	Supported
System Controller & autodetect	Supported
Geographic Address	Supported

Features	Compliances
Master/Slave cycle with user AM	Supported
Configuration Space	ANSI/VITA 1-1994 supported. customizable to other non standards
User non stand. bus signal	Supported (customizable)
ANSI/VITA 23-1998 (VME64xP) CBLT e MCST cycles	Unsupported
ANSI VITA 1.5-1999 & VME64X 2eVME 2eSST cycles	Unsupported

Ordering Information

The main existing boards and IP configuration are listed below, others combinations are in the other specific datasheet or can be created according to the customer requirements.

Product Name	GEB Code	Description
VME-N-A32D32	111120A7	Master/Slave Srinked Board, 2xRS232 (Hardware Only) without GEB Front [*2].

Notes

- [*1]: FEWE is the Fpga Easy Web Editor, demo is currently available at: http://www.geb-enterprise.com/Hidden_Pages/Fpga_System_Edit_and_Configure.html
- [*2]: The partnumber includes license of caming so on FEWE and of the all VME SMILE Templates.

GEB Enterprise S.r.l.
General Electronics Business
Via Rocca di Papa, 21 –00179 Roma, Italy
Phone: 06 7827464 Fax: 06 7806894
Email: info@geb-enterprise.com
Web: www.geb-enterprise.com