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General Electronics Business

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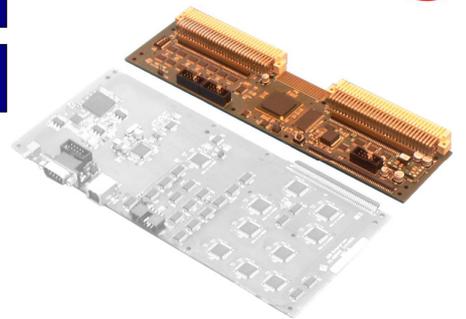
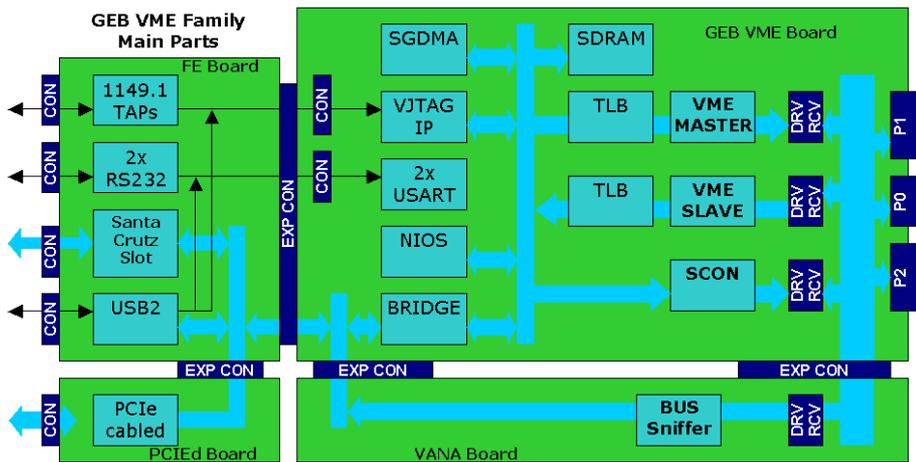
VME-RDK

System On Programmable Chip

VME BUS Rapid Development Kit

Overview

The VME Bus family has the target to make available at low cost the resources to build a fast prototype of a VME master/slave/controller subsystem. The modularity of the resources, both hardware board and firmware VHDL IP allow to compose **many types of application with a low effort**.



The application field may be:

- In heterogeneous systems, when you wish to make a **system soft growth up**, a mixture of different form factor boards and a flexible bridge could be needed, for instance between PC/PXI bus and VME standard/customized bus.
- In components or boards obsolescence replacement. To save money, the VME IP can include a bus interface able to emulate the local bus timing of obsolete solution that You are replacing.
- In test systems to perform test cycles to UUT slave board and/or to acknowledge bus cycles from an UUT master board and to perform bus signals check at same time.

The GEB-VME board hosts the Fpga, that makes available the modular VME IP, the VME Drivers and Receivers, SdRam and Fpga ancillary logic, including a switching power supply, able to generate onboard 3V3 when it isn't available on the P0 connector. The board is built in two classes of form factors.

- The first one **has a standard high 6U** but the length was reduced to 58mm to allow the connection with a "front end" board that will host additional resources such as I/O interfaces or access ports. The front end board will be vigorously joined together the GEBVME board using 4 smalls brackets and a 100 ways, 1.27mm pitch smt connettor, that allow to use Fpga I/O signals to make specific interface applications.



VPC-QP192-BS
Full custom VME board, Virginia Panel QuadraPaddle Connector, size 142x108mm

- The second class **is a non-standard, customized small size form factor** thought to be used inside **customized (special) VME bus format**, such as:
 - **Military** versions of VME bus (MCS Bus)
 - High performance test equipment where a VME master/slave controller equipped with Virginia Panel interface connector make it very useful

This kind of application often requires both custom form factor and special dedicated signals, like System fail status, System On line, triggers, syncs and so on that can be simply supported using fpga I/O signals together with small VHDL code improvement.

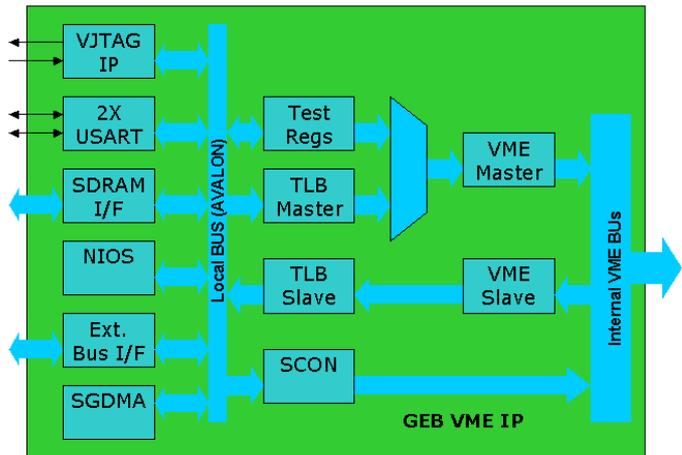


Full custom, MCS child board, size 83x108mm

The default VME-IP and firmware support A32D32 master/slave cycles interrupt handler, interrupter and SysCon. The related firmware (Monitor), running on NIOSII, allows the user to start all kind of bus cycles and some macro commands, such as memory test, using RS232 or USB data link.

VME IP Architecture

The IP Architecture allows the user to build many VME board structures. Building the user system is very simple: the local IP Bus is compliant to the Altera SOPC/QSYS specifications, allowing the users to make the FPGA subsystem using the Altera tools. The TLB Master Block allows the address translation from a local address to a Vme address using an addressing space of up to six different VME addresses. The TLB Slave Block allows the translation from a max of six Vme addresses to a local address. A special addressing space, configurable at compilation time, allows the programming of slave TLB from VME bus, opening the internal registers, including TLB Master and SGDMA, to be programmed by standard VME cycles. Some test registers allows access to all VME space without programming the master TLB, simplifying the access to VME resources during debug and test operations. The VJTAG IP can be used to access to all resources, internal and external (VME). This function allows BSCAN test operation using BSCAN tools, such as Jtag Technologies Provision and Jtag Functional Test (JFT).

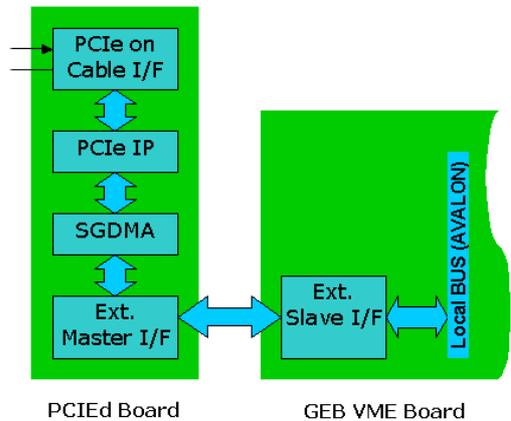


The External Bus I/F makes available a logical connection between the FPGA I/O pins and the internal Avalon bus. Two types of external bus I/F can be used:

- External Slave I/F, that will be an Avalon Master, allows an external master (USB, PCIe and so on) to access to internal resources. This function was designed to build bridge from an external Host (also with different form factor such as PC, LapTop, PXI and so on) and VME peripherals.
- External Master I/F, that will be an Avalon Slave, allows the internal master (NIOS, VJTAG, VME Slave I/F) to access external slave resources. This function was designed to build user custom interface controlled from VME bus and/or local NIOSII processor.

Currently there are some available EXT Bus I/F that allow:

- The highest performance data link to a lot of different form factor hosts (LapTop, Std PC, PXI PC, Rack PC, SBC) through the PCIe on cable interface.
- The medium one, with highest flexibility data link to a lot of different form factor hosts through an USB interface.
- GPIO, General Purpose Interface Parallel I/O, that can used in evaluation phase.



Different custom version of external interface for specific application can be developed by GEB or by user, using Altera's tools such as QuartusII, SOPC Builder and QSYS.

Application, Standard types card

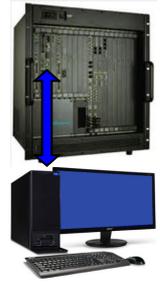
The flexible IP architecture makes available the following standard VME Board structures:

- Silly Slave, the simplest VME card structure, many I/O resources, normally slow, with an optional local DMA (just from local resouces and local memories).
- Smart Slave, a simple VME card structure, many I/O resources, normally slow, with on board processor and with an optional local DMA.
- Silly Master, a powerful structure, a lot of I/O resources, normally fast, with chained DMA controller able to transfer data from local registers to local memory or VME memory or between local memory and VME memory
- Smart Master, the most powerful structure, adds to the capability of Silly Master structure a local NIOSII processor, able to manage the DMA queue, interrupts and so on.

Application, Systems Upgrade

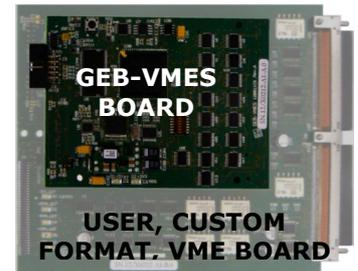
In life cycle of systems, in order to fight competitors, some improvements may be required to increase performance or to open the system to new standard interfaces, without redesigning all system hardware and software, rather than a soft and progressive upgrade allows to sell the upscale to existing customers. This could be done using VME Master Board together with a PCIE on-cable interface board that consents:

- High speed data transfer between an external computer and the VME resources.
- Use of an external computer able of powerful coprocessing, equipped with state of art interfaces, such as Gigabit Ethernet and USBIII.
- The Improvement of VME bus performance, using Block Transfer just where it will make significative changes on system performances (See next application)



Application, VME Board Custom format

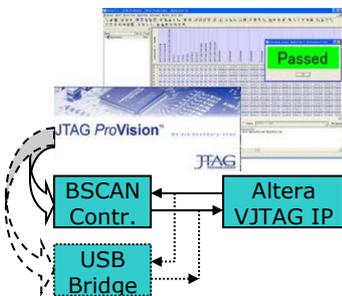
This kind of application is dedicated to special VME systems, such as military and test equipment. This type of application is strictly related to the previous application. Some board upgrades could be needed during an upgrade of an existing system where you wish to increase the performances of several functions. Often an existing design is based on obsolete VME solutions, such as some CPLD that interface the VME to a local bus. A redesign, using state of art devices, such as a Tundra, would probably be strongly complicated because the internal bus of the board, normally, isn't a standard bus supported by currently VME interface devices. The GEB-VMES (GEB-VME board Shrunked) is a good solution: it includes the whole VME interface (FPGA, drivers, receivers and so on) in a small size (about 83x108mm), allowing the users to ignore all VME requirements. It also offers, on the expansion connector, an interface that will be tailored to emulate the local protocol of an existing design; that makes very simple the obsolete custom card redesign:



- Removing the out of date VME interface.
- Adding the interface connector, using its I/O signals to connect the local bus and the EXT-IF IP together.
- Customizing the EXT-IF VHDL code to manage data transfer between local and Avalon bus. That could be done by yourself or by GEB.

If you wish, GEB-VMES board schematic and FPGA could be bought and directly inserted inside your design, avoiding a two boards sandwich.

Application, BSCAN and Functional Testing



BSCAN tools and Altera VJTAG IP can be used to access to all resources, such as registers or memories, onboard and on VME Bus. This function allows BSCAN test operations at test speed using BSCAN test tools, like Jtag Technologies Provision, or generate single VME cycle at full speed, using Jtag Functional Test tools, such as Jtag Technologies JFT (Python Language). Using the resident firmware (on NIOSII) along with JFT, the user can generate full speed test sequences, including blocks transfers, memory fill and check, etc. The interface between the BSCAN tools could be done through a standard 1149.1 TAP connector using a high performance external BSCAN controller or through an USB2 port using an onboard, embedded, medium performances BSCAN controller. The used controller is fully transparent to the test software developed using Jtag Technologies PROVISION or JFT. The size of GEB VME

board allows the user to put it inside an enclosure (2U high) and the UUT on the top side allowing easy access to top and bottom side for trouble shooting operations.

Application, VME sniffer

An optional daughter board, GEB VANA, allows the storing of VME bus cycles in state mode and/or in timing mode. An Input/Output external trigger can be used as an input to trigger storing or, as an output, to trigger an external instrument (i.e. Oscilloscope). Using USB or RS232 or 1149.1 Bscan Tap, the sampled data can be stored on a small and fast memory: in high speed timing mode on fpga memory (up to some Kbytes), or in state mode on a onboard memory buffer (up to some Mbytes). Using the PCIe on cable interface the sampled data could be stored in a very huge buffer using host system memory or disks. For Example, assuming 2 Mbytes/Sec average VME bus data rate:

- Using 2Gbytes system memory, up to 30Minutes of data bus activity can be memorized.
- Using 1Tbyte disk space, up to 23 Days of data bus activity can be stored.



Application, Obsolescence solutions, VME ASIC replacement

The VME IP can be fitted in a small size BGA FPGA and can be hosted on apposite PCB carrier to replace, pin to pin, obsolete VME ASICs. The VME IP has been designed to obtain the maximum flexibility in the replacement of ASIC. In fact, a lot of obsolete ASIC designs have been made on the border between VME Rev.C and VME64 specs; in these ASICs could have included some non standard extensions that weren't frozen in VITA specs that were changing at design time. **Some typical non-standard extensions where something changed could be:**



- Geographic Address.
- Address space configuration registers, using user defined Address Modifiers (An ancestor of CSR whose definition began in VME64 specifications).

Related Boards

PCI Express External Cabling. PCI Express Cable is a standard developed by the PCI-SIG to transmit the host PCI Express bus over a high-speed cable. This can be done internally to a system enclosure or externally in a box-to-box type application. Using a PCIe cable is possible to extend the PCI Express bus up to seven meters from the host CPU complex and without any circuitry for suppressing the inherent noise. The PCIe Cable allows splitting the host PCIe environment by the remote embedded I/O subsystems, also using different form factors.



Compliance Levels

Features	Compliances
A32,A24,A16 Addressing Spaces	Supported
D32,D16,D8E,D8O Data Transfer	Supported
Master/Slave Block Transfer D64, D32, D16	Supported by hardware (Optional IP version)
Interrupter, Interrupt handler	Supported
System Controller & autodetect	Supported
Geographic Address	Supported

Features	Compliances
Master/Slave cycle with user AM	Supported
Configuration Space	ANSI/VITA 1-1994 supported. customizable to other non standards
User non stand. bus signal	Supported (customizable)
ANSI/VITA 23-1998 (VME64xP) CBLT e MCST cycles	Unsupported
ANSI VITA 1.5-1999 & VME64X 2eVME 2eSST cycles	Unsupported

Ordering Information

Main existing boards and IP configuration are listed below; other combinations are in the other specific datasheet or can be created according to the customer requirements.

Product Name	GEB Code	Description
VME-BRG	111120A1	A32D32 Scon/Master/Slave Board, Front End with RS232, 1149.1 Tap, custom version
VME-A32D32	111120A2	A32D32 Scon/Master/Slave Board, Front End with RS232, USB, 1149.1 Tap.
VME-S-A32D32	111120A3	A32D32 Scon/Master/Slave Board, Sniffer, RS232
VME-U-A32D32	111120A4	A32D32 Scon/Master/Slave Board, Sniffer, RS232 and USBII Interface
VME-B-A32D64	111120A5	A32D64 Scon/Master/Slave Board, D64 Block Transfer, Front End with RS232, USB, 1149.1 Tap interfaces with USB Bridge
VME-P-A32D32	111120A6	A32D32 Master/Slave Board, Front End with RS232, USB interfaces, PCI Express Downstream Interface
GEB-VMES	120811A1	Master/Slave sripped Board, 2xRS232 (Hardware Only)
VMS-A32D32	130313A1	Master/Slave sripped Board, 2xRS232, default VME-IP and Firmware (Monitor)
VMS-A32D32	130313A2	Master/Slave sripped Board, 2xRS232, default VME-IP, FEWE compliant I/O and Firmware (Monitor)
VPC-QP192-BS	160117A1	A32D32 Scon/Master/Slave Board, with RS232 and USB I/F, 1149.1 Tap, Virginia panel version with QuadraPaddle 192 pins connector.



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