



GEB Enterprise S.r.l.

General Electronics Business

Via Rocca di Papa, 21 - 00179 Roma, Italy

Email: info@geb-enterprise.com - Web: www.geb-enterprise.com

VPC-QP192-BS VME TESTER BOARD on VIRGINIA PANEL

Overview

VPC-QP192-BS is VME compliant board has been designed to be hosted in test system that uses in the Virginia Panel interconnection system. The board is equipped with with Virginia Panel QP192 connector, an Intel (Altera) Fpga, 1xRS232 Interfaces, Local DRAM, 1149.1 Jtag TAP. The onboard firmware makes available a set of simple command, such as VmeRead or VmeWrite with many addresses and data modes, or complex commando such as memory tests.

Features

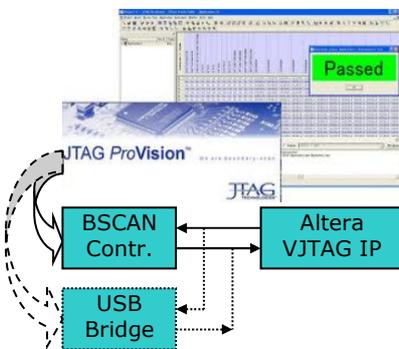
The FPGA VME logic includes the following Capabilities:

- VME Master interface A32-A24-A16, D32-D16-D8E-D8O
- VME system controller
- VME slave interface, A32-A24-A16, D32-D16-D8E-D8O
- VME Interrupter
- VME Interrupt handler
- Standard and Special (Custom) configuration space master and salve capability
- DRAM Controller
- NIOS CPU with User Monitor allows test commands from RS232/USB
 - Simple Read and Write cycles, including interrupt acknowledge cycles
 - Complex Macro command such as Memory tests.



Application, Functional and BSCAN Testing

The VPC-QP192-BS board can operate in a test environment can operate both in functional both in BSCAN mode.



In functional test mode, command and response can be managed by RS232 or USB interfaces. The on board MPU will decode the command, will perform the actions, and will send back the results. Commands can be oriented to do simple operation, such as VmeReadm VmeWrite or VmeCheck, or complex, such as Memory tests. Both of them can be performed at 8, 16 o 32 bits. Some low level command are dedicated to interrupt handling, they can be used to generate interrupts, check interrupt status, and perform interrupt ack cycles at any level. API to interface VPC-QP192-BS commands to common used tests enviroments are available. Special cycles, with user defined address modyers, are allowed to perform to initialization of VME modules configuration space.

BSCAN tools and Altera VJTAG IP can be used to access to all resources, such as registers or memories, onboard and on VME Bus. This function allows BSCAN test operations at test speed using BSCAN test tools, or generate single VME cycle at full speed, using Jtag Functional Test tools, typically written in Python Language. The interface between the BSCAN tools could be done through a standard 1149.1 TAP connector using a high performance external BSCAN controller or through an USB port using an onboard, embedded, medium performances BSCAN controller.

Board and Fpga architecture

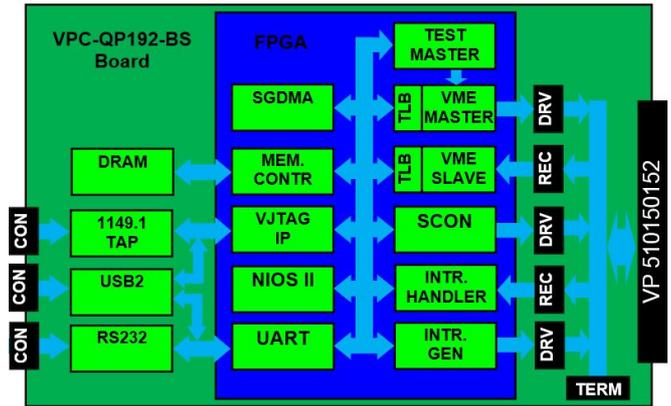
The GEB-VME board hosts the control logic in an Fpga; it makes available the modular VME IP, granting large flexibility and growthly if this will be neededmto in the user test application. The board hosts the vme buffers and receiver fully compatible with vme driving capability, being the board to one ends of the bus the default configuration host the VME termination

The board hosts a Sdram that can be used how target in vme slave cycles, the slave address translation block (TLB), windows base address and size registers (BARS) allow allocation of local Sdram everywhere in Vme addressing space.

Test Master is a bus cycles generator that allows an indirect access, through the VME Master, to everywhere in VME Addressing space. Consequently, due to a test commands, the vme bus parameters will be stored in some registers before start the cycle.

Areas in Vme addressing space can be locally mapped through the Master TLB, consequently the NIOS Cpu can access directly in a VME memory area, without reprogramming any registers, at its full speed, gaining the capability of perform memory tests at high speed.

The interrupter function can activate any one of the seven available interrupt lines and can accept interrupt acknowledge at correspondent IPL, giving back the interrupt vector. The vector can be programmed in a register.

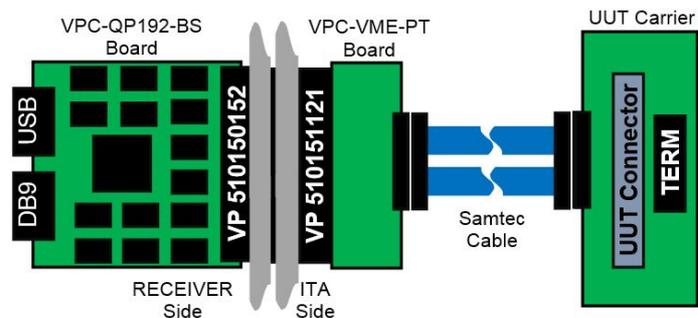


The interrupt handler function is able to read the status of the interrupt lines, making it available to Interrupt read status commands. The interrupt handler can also perform interrupt acknowledge cycles at any IPL level to reset interrupt source and get its vectors.

The VPC-QP192-BS board supports non-standard VME cycles also, it, using some user defined Address Modifiers, is able to address non-configuration registers implemented in some special functiobs board. This metohd is an ancestor of CSR whose definition began in the VME64 specifications, it's used sometime in some VME derived bus, such as the avionic MCS bus.

VPC-QP192-BS to UUT connection

Typically, the UUT will be inserted on a board that hosts a motherboard connector set. One termination has been fitted on the VPC-QP192-BS board; the second one must be fitted close to the UUT connector.



The test fixture ITA side must interfaces with a VP 510151121 connector generally places on a passive transition board. Regarding the cable needed to reach the UUT carrier bust, take care to the impedences will be duty. A standard VME tracks have an impedance of 100 ohm when unloaded, under 50 ohm when full loaded. Using of 50-ohm, high density, shielded cable, like Samtec HQCD, will be a good idea. A transition board named VPC-VME-PT can be supplied on request.

Compliance Levels

Features	Compliances
A32,A24,A16 Addressing Spaces	Supported
D32, D16, D8E, D8O Data Transfer	Supported
Master/Slave Block Transfer D64, D32, D16	Supported by hardware (Optional IP version)
Interrupter, Interrupt handler	Supported
System Controller & autodetect	Supported
Geographic Address	Supported

Features	Compliances
Master/Slave cycle with user AM	Supported
Configuration Space	ANSI/VITA 1-1994 supported. customizable to other non standards
User, non-standard, bus signal	Supported (customizable)
ANSI/VITA 23-1998 VME64xP CBLT e MCST cycles	Supported by hardware (Optional IP version)
ANSI VITA 1.5-1999 & VME64X 2eVME 2eSST cycles	

Ordering Information

Product Name	GEB Code	Description
VPC-QP192-BS	160117A1	A32D32 Scon/Master/Slave Board, with RS232 and USB I/F, 1149.1 Tap, Virginia panel version with QuadraPaddle 192 pins connector.
VPC-VME-PT	180299A1	Vme Virginia Panel Pass Throught Board



GEB Enterprise S.r.l.
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 Via Rocca di Papa, 21 -00179 Roma, Italy
 Phone: 06 7827464 Fax: 06 7806894
 Email: info@geb-enterprise.com
 Web: www.geb-enterprise.com

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